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EXAMINER

NGUYEN, HAU H

ART UNIT PAPER NUMBER

2628

DATE MAILED: 09/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

DETAILED ACTION

The response filed 7/20/2006 have been considered in preparing this Office action.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 5-9, 11-20, 22, 23, 26, 27 and 30-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al (U.S. 5,696,940 hereinafter "Lin") in view of Chekerylla (U.S. 6,084,598).

Lin teaches a method of increasing image processing performance by explicitly copying a first instance (The words "first instance" can be broadly interpolated as just the first data being transfer from I/O memory to the main memory) of an image data (the input data from the I/O device 22 can be a video camera for capturing an image, a video monitor, printer, network port, etc, see col. 2, lines 40-41) between a buffer (not shown, but would have been obvious to include as suggested by Bowes in order to temporarily store the data before it is written to its destination, see col. 1, line 63 to col. 2, line 4) in main memory (Fig. 1, main memory 14) and an I/O memory (RAM 20; it is noted that Lin does not particularly called the RAM 20 an I/O RAM, however, the RAM 20 is used for storing the input data from the I/O device 22 before transfer into the main memory 14 and thus can be called an I/O RAM, see col. 1, lines 18-21. Lin further teaches a FIFO

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buffer within the RAM 20 to store the input data from the I/O device 22) by a DMA circuitry (18) that controls data transfers between the main memory (14) and I/O RAM (20). Lin further teaches a CPU (12, it is noted that any CPU made or on the market at the time of this invention at least includes the functionality of performing any kind of basic "CPU intensive operations" for a PC or any well known "host computer") can read data from main memory (14) and write the processed result into the main memory 14. However, Lin fails to explicitly suggest or teach "explicitly copying a first instance of an image into a second copy of said image in a buffer in the memory".

However, this is what Chekerylla teaches (Figs. 1 and 6, and col. 6, lines 13-21, and col. 8, lines 39-42). Chekerylla also teach the CPU access is made directly to the extra second copy of the data in memory and not to the first instance in said I/O RAM. Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Chekerylla in order to enhance image manipulation without changing the original image (col. 17, lines 23-36).

For at least the above reasons, claims 1, 5, 12-18, 22, 23, 26, 27 and 30 would have been obvious.

As per claims 6-9 and 31-33, the combined system teaches how the image data is being copied (e.g. Chekerylla, as the CPU calls for the graphics application 113 in Fig. 6).

As per claim 11, Lin fails to explicitly teach said I/O RAM is associated with a video digitizer. However, if the I/O device 22 is a video camera, a video digitizer would have been obvious to include if not inherent to in order to digitize the captured image.

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As per claims 19 and 20, although Lin fails to teach the processor executes programs to enhance, compress/decompress, encrypt/decrypt, or reformat said image data, Chekerylla teaches the processor executes programs to enhance image (for example, smoothing image 202).

3. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al (U.S. 5,696,940 hereinafter "Lin") in view of Chekerylla (U.S. 6,084,598) as applied to claim 1 above, and further in view of Anderson et al (U.S. 6,338,119, hereinafter "Anderson").

The teachings of Lin and Chekerylla are given in previous paragraph of this Office action. However, the combined system fails to explicitly teach a L1 and L2 cache memory. It was old and well known and well used in the art to include a L1 and a L2 cache memory in order to speed up the system processing by access data locally from the cache instead of main memory. Furthermore, Anderson teaches a L1 (Fig. 1, 104) and L2 (106) cache memory. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Wada or Anderson into the combined system of Lin and Bowes in order to provide fast access to the storage device and thus improves the overall system performance because a cache is a much faster storage device than any other RAM for the CPU or other computation device. Therefore, at least claims 2-4 would have been obvious.

4. Claims 21, 24, 25, 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al (U.S. 5,696,940 hereinafter "Lin") in view of Chekerylla (U.S.

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6,084,598) as applied to claim 16 above, and further in view of Cullen et al (6,592,629 hereinafter "Cullen").

The teachings of Lin and Chekerylla are given above. However, the combined system fails to explicitly teach said processor executes programs to enhance, compress/decompress, encrypt/decrypt, or reformat said image data. These are what Cullen teaches. Cullen teaches remote document image storage and retrieval system for a multifunctional peripheral comprising a workstation (630) and a multifunction machine (140) includes a compress/decompress (252), an encrypt (253) and decrypt (254). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Cullen into the combined system of Lin and Chekerylla in order to reduce overall storage space and provide fast and secure transmitted over the bus or network as taught by Cullen (col. 5, lines 16-63). Therefore, at least claims 19, 20, 24, 25, 28 and 29 would have been obvious.

Claim 21 is similar in scope to the combination of claims 1, 11, 12 and 19-20, and thus is rejected under similar rationale.

Response to Arguments

Applicant's arguments with respect to claims 1-9, 11-33 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion


5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is (571) 272-7787. The examiner can normally be reached on 8:30am-5:30pm Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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H. Nguyen

9/25/2006



KEE M. TUNG
SUPERVISORY PATENT EXAMINER